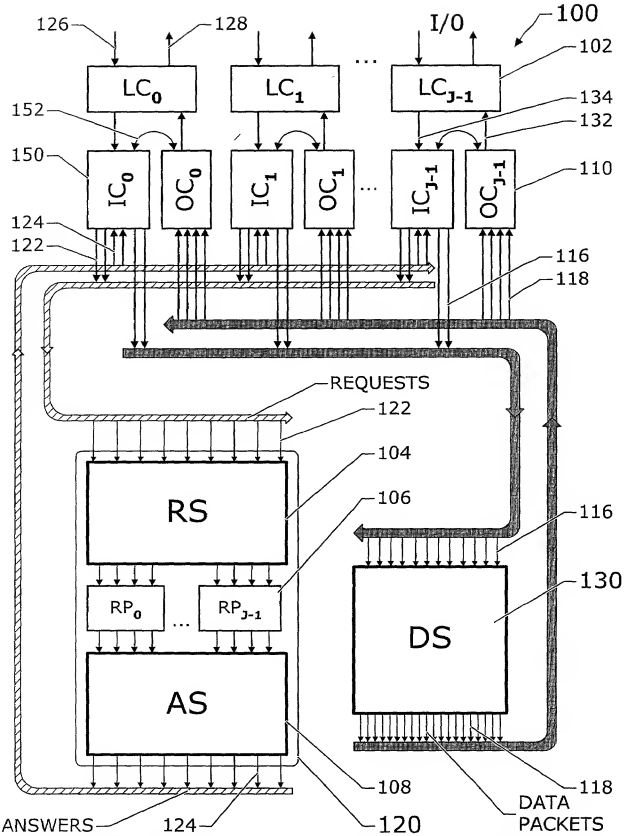


CONGESTION-FREE SWITCH SYSTEM

Fig 1A

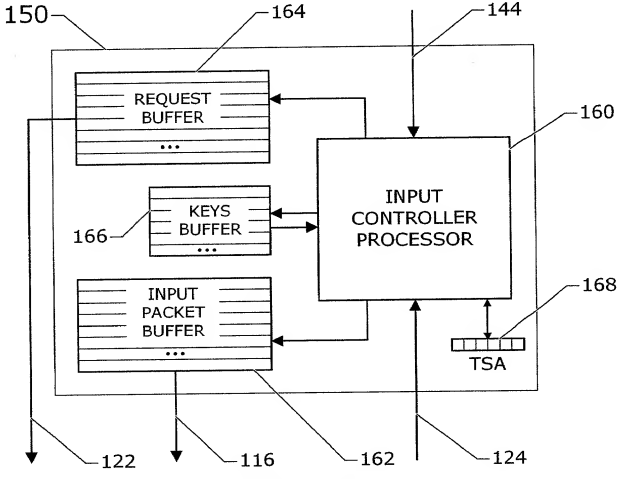


Fig 1B

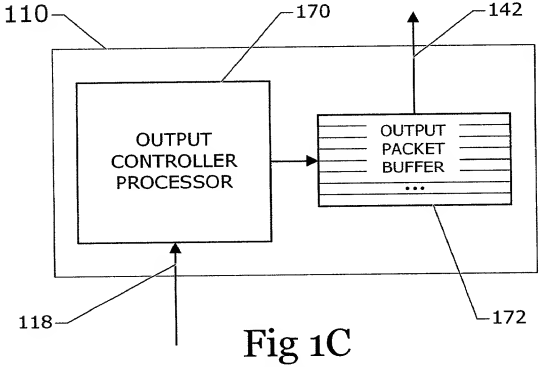
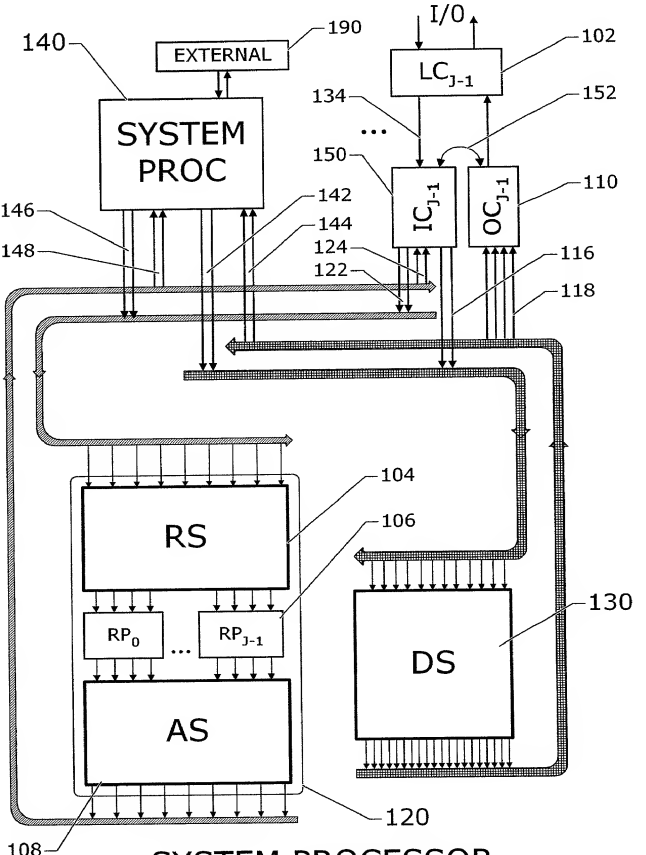


Fig 1C

INPUT AND OUTPUT CONTROLLERS



SYSTEM PROCESSOR

Fig 1D

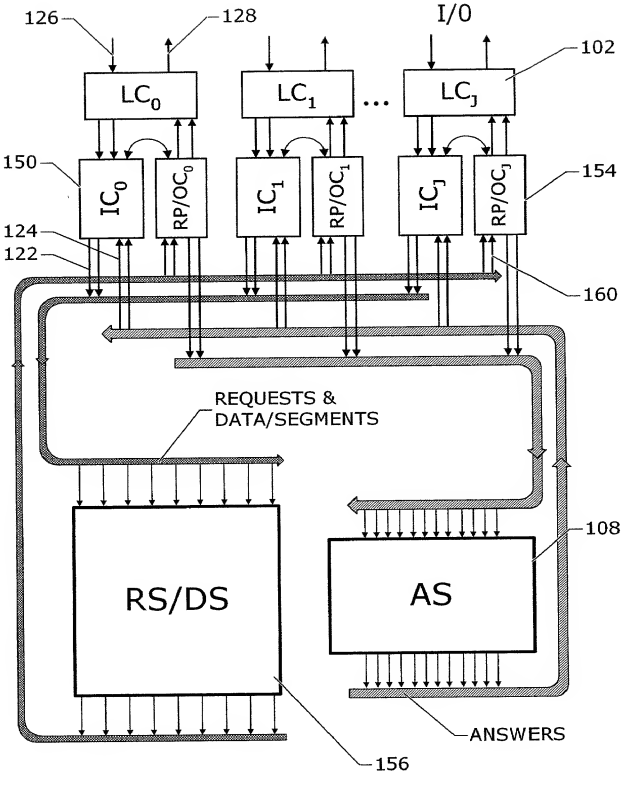

126
128
I/0
102
LC0
LC1
...
LCJ
150
IC0
RP/OC0
IC1
RP/OC1
ICJ
RP/OCJ
154
124
122
160
REQUESTS &
DATA/SEGMENTS
108
RS/DS
AS
ANSWERS
156

Fig 1E

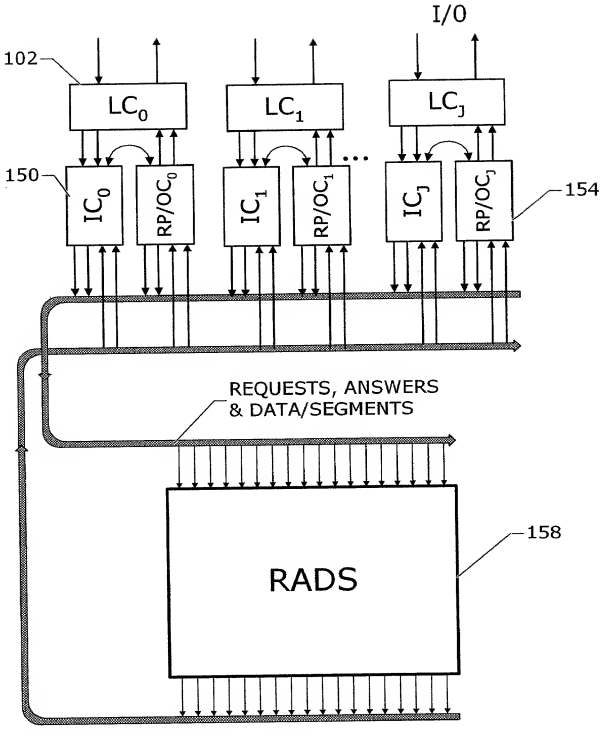


Fig 1F

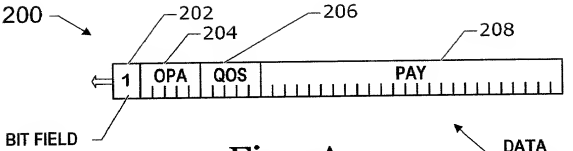


Fig 2A

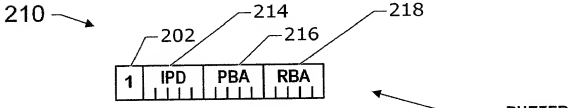


Fig 2B

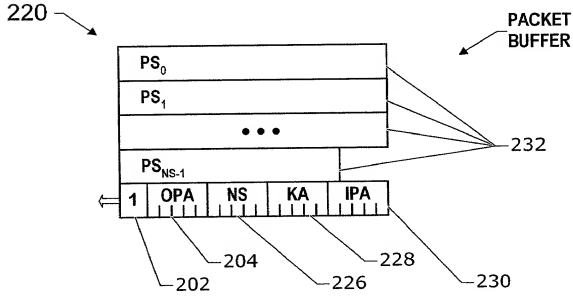


Fig 2C

PACKET FORMATS AND LAYOUTS

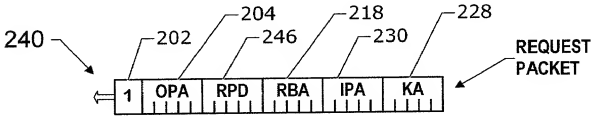


Fig 2D

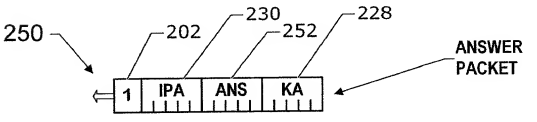


Fig 2E

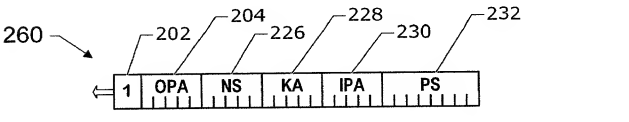


Fig 2F

PACKET FORMATS AND LAYOUTS

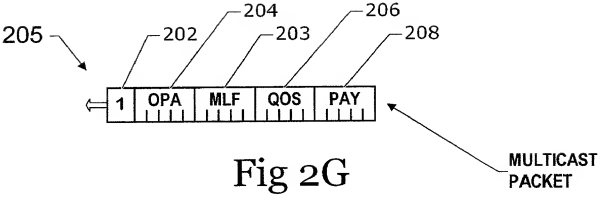


Fig 2G

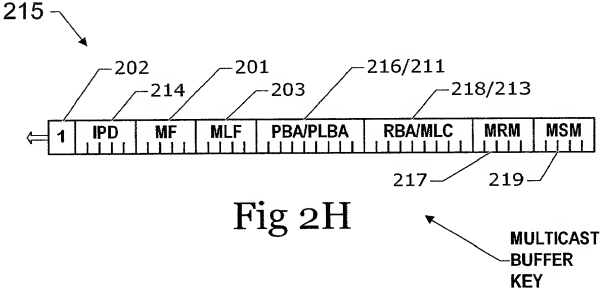


Fig 2H

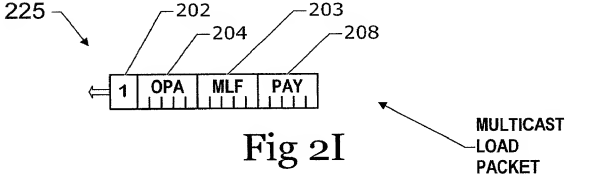


Fig 2I

PACKET FORMATS AND LAYOUTS

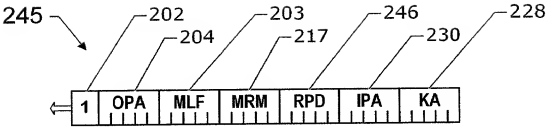


Fig 2J

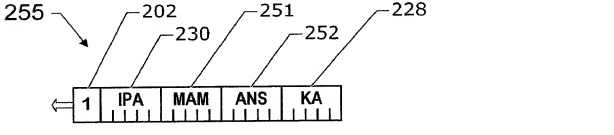


Fig 2K

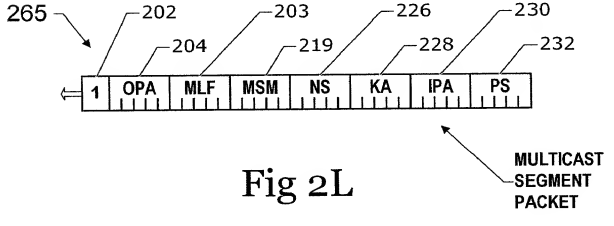


Fig 2L

PACKET FORMATS AND LAYOUTS

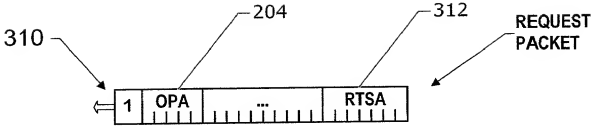


Fig 3A

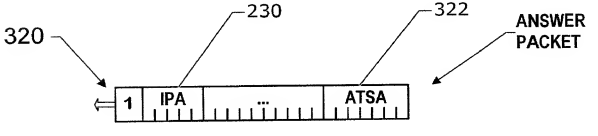
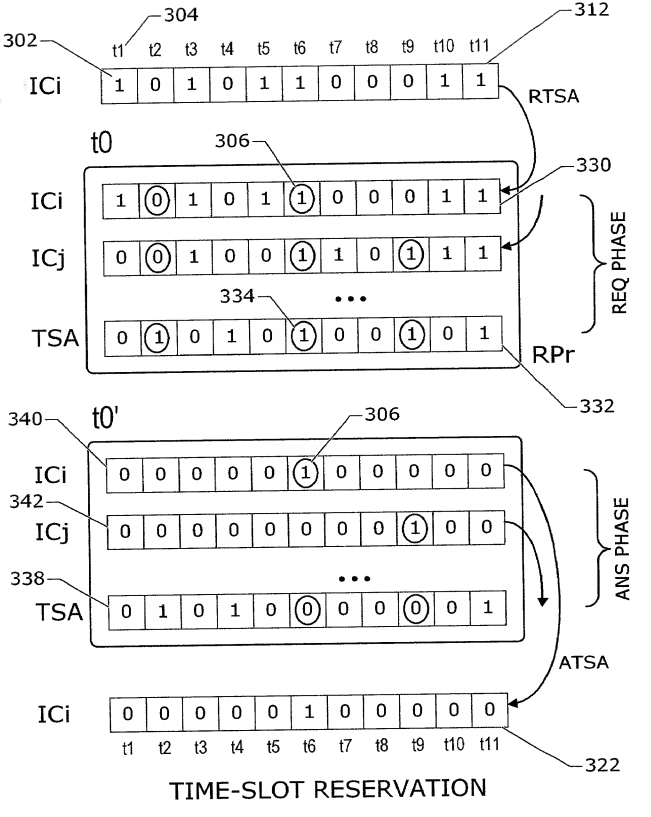


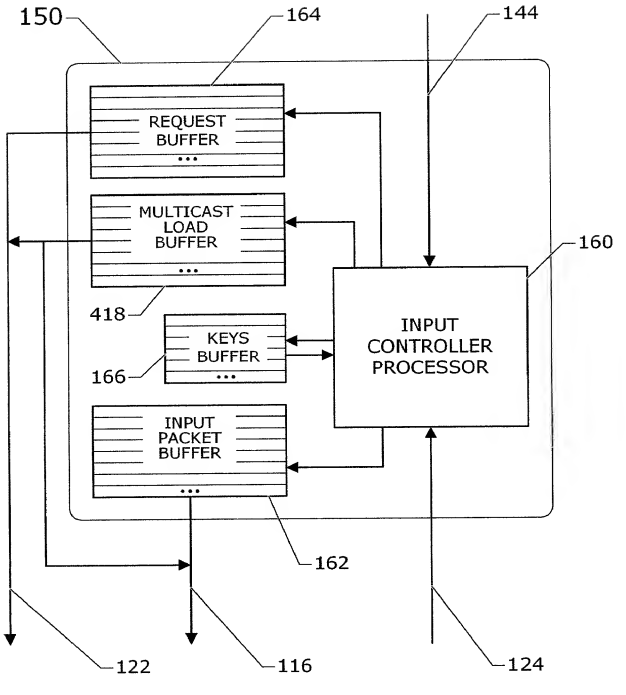
Fig 3B

PACKET FORMATS AND LAYOUTS



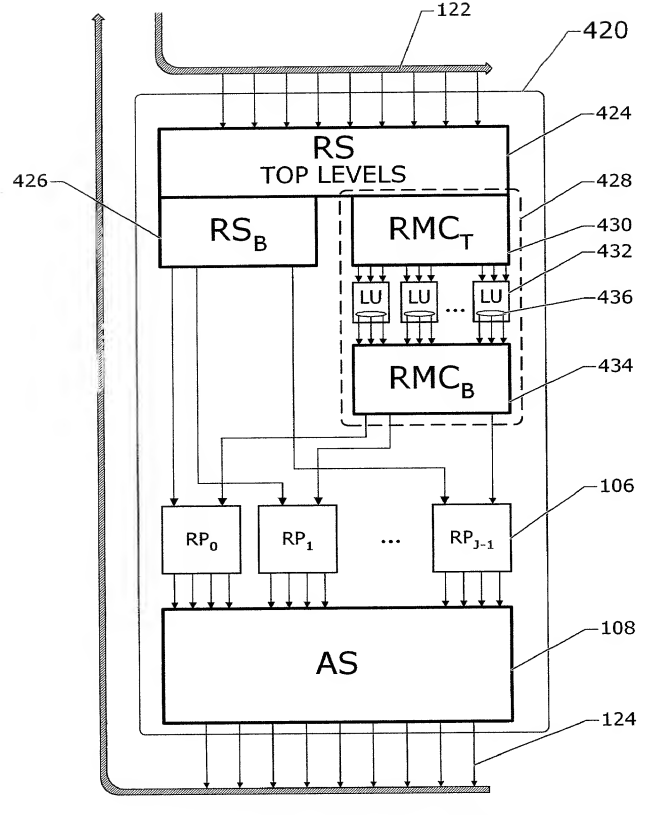
TIME-SLOT RESERVATION

Fig 3C



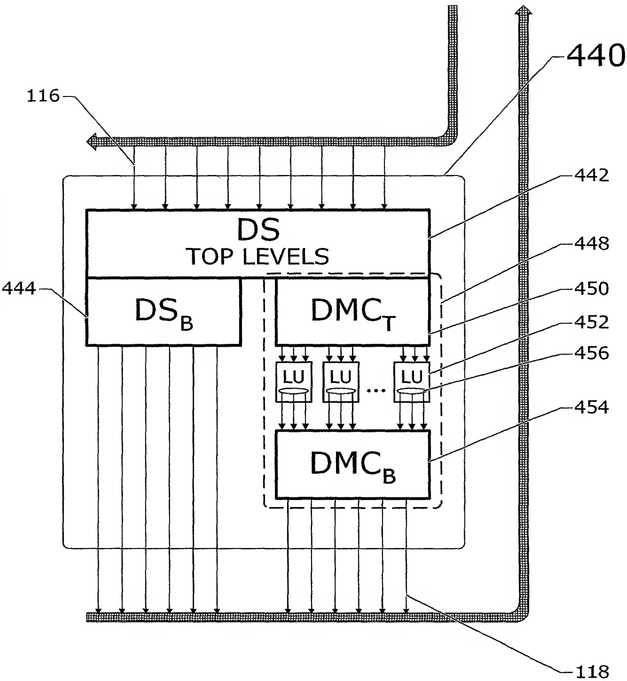
MULTICAST INPUT CONTROLLER

Fig 4A



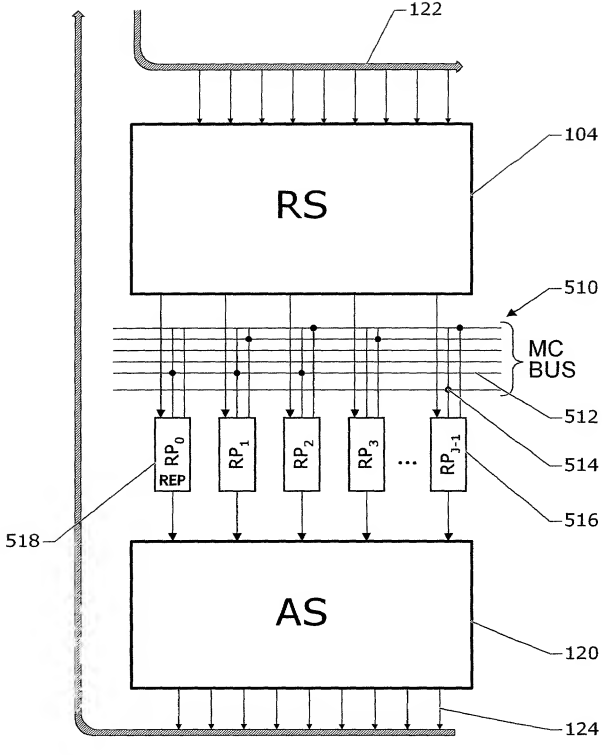
MULTICAST CONTROL SYSTEM

Fig 4B



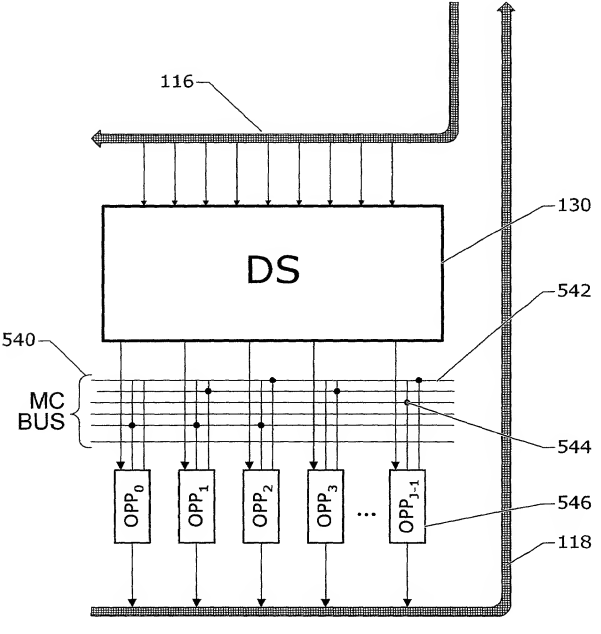
MULTICAST DATA SWITCH

Fig 4C



MULTICAST BUS CONTROL SYSTEM

Fig 5A



MULTICAST BUS DATA SWITCH

Fig 5B

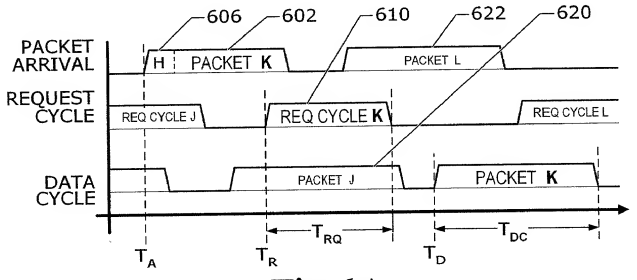


Fig 6A

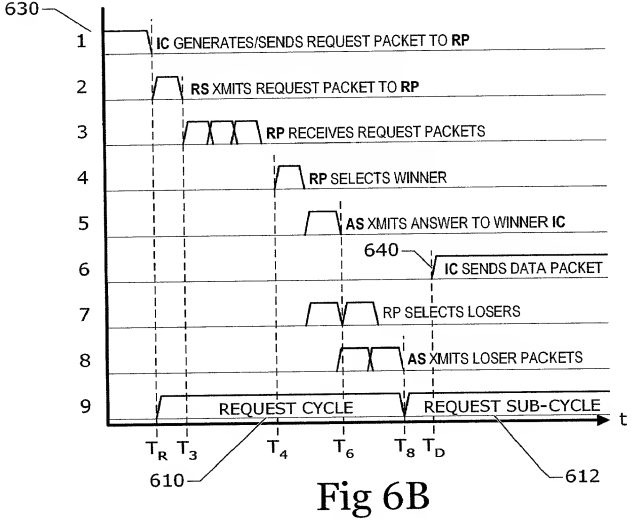


Fig 6B

CONTROL AND DATA CYCLE TIMING

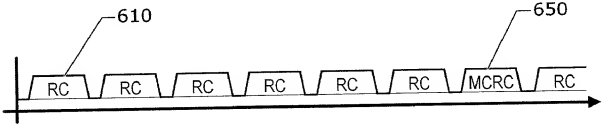


Fig 6C

MULTICAST CONTROL CYCLE TIMING

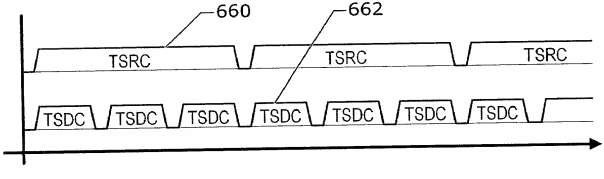
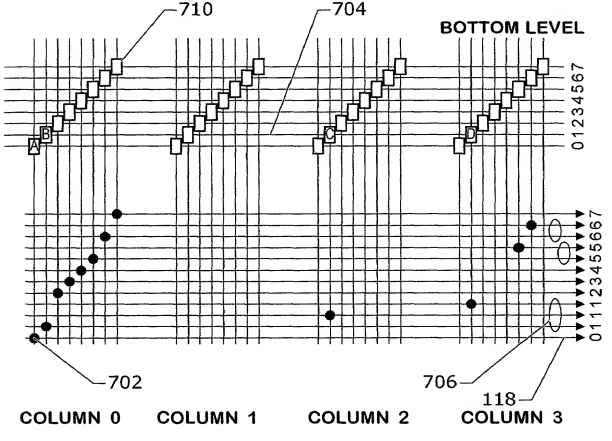


Fig 6D

TIME-SLOT RESERVATION TIMING



CONFIGURABLE OUTPUT

Fig 7

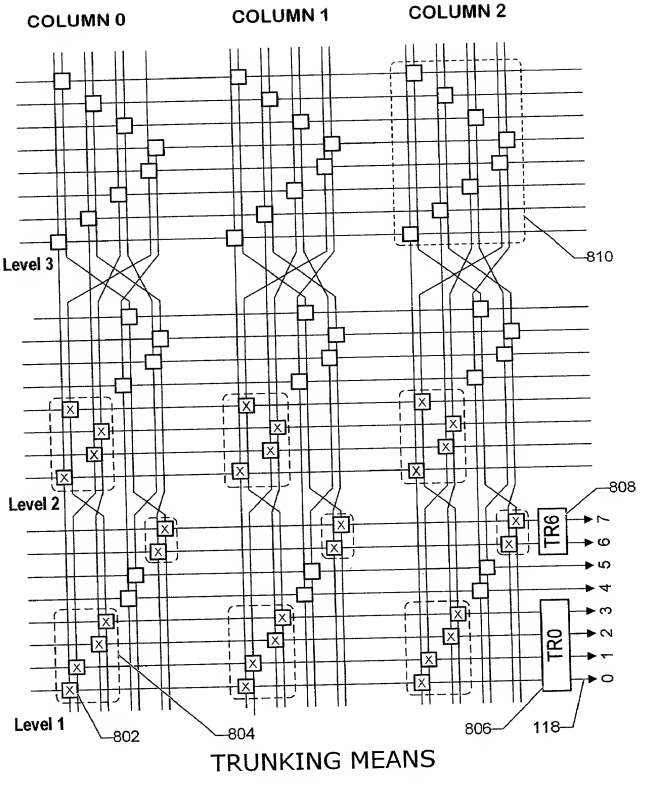
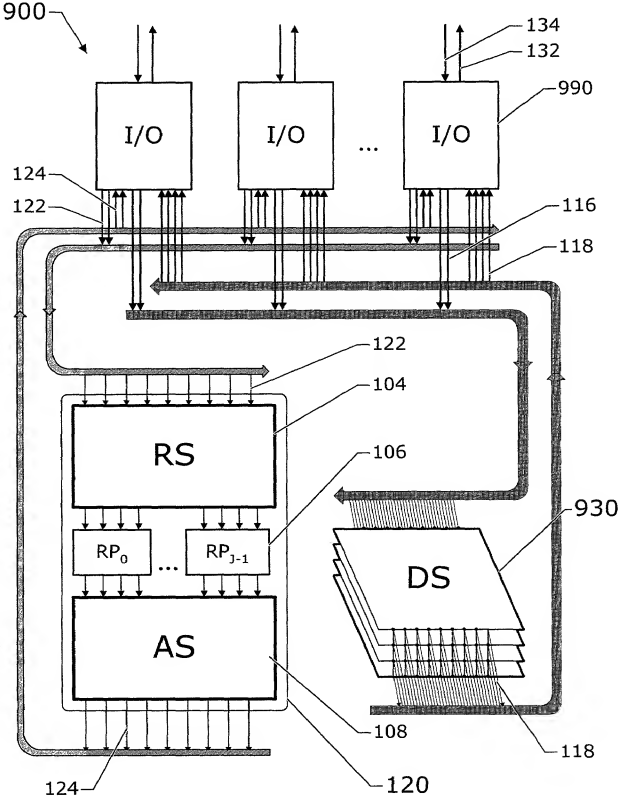

COLUMN 0
COLUMN 1
COLUMN 2
Level 3
Level 2
Level 1
810
808
TR6
TR0
0 1 2 3 4 5 6 7
802
804
806
118
TRUNKING MEANS

Fig 8



PARALLEL DATA SWITCH

Fig 9

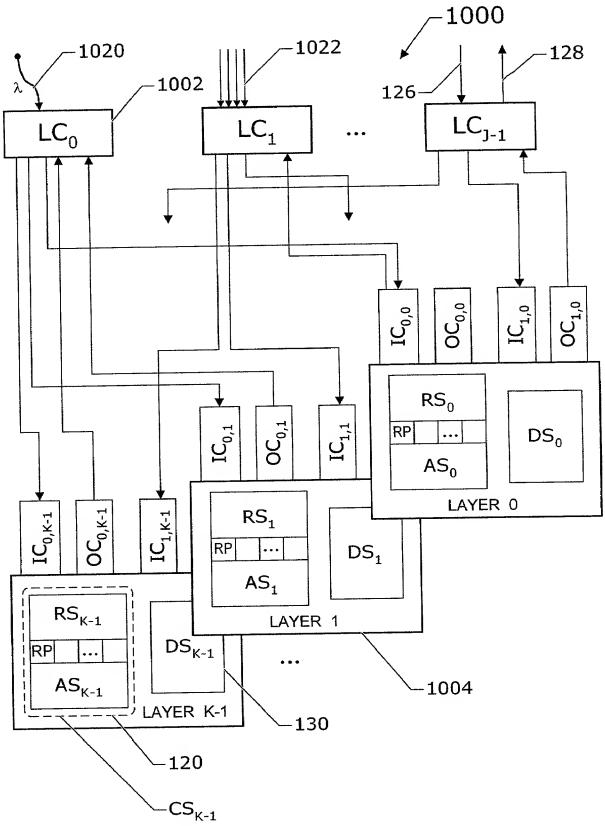

1000
1020
1022
128
126
1002
λ
LC0
LC1
...
LCJ-1
IC0,0
OC0,0
IC1,0
OC1,0
RS0
RP
...
AS0
DS0
LAYER 0
IC0,1
OC0,1
IC1,1
IC0,K-1
OC0,K-1
IC1,K-1
RS1
RP
...
AS1
DS1
LAYER 1
RSK-1
RP
...
ASK-1
DSK-1
LAYER K-1
1004
130
120
CSK-1

Fig 10A

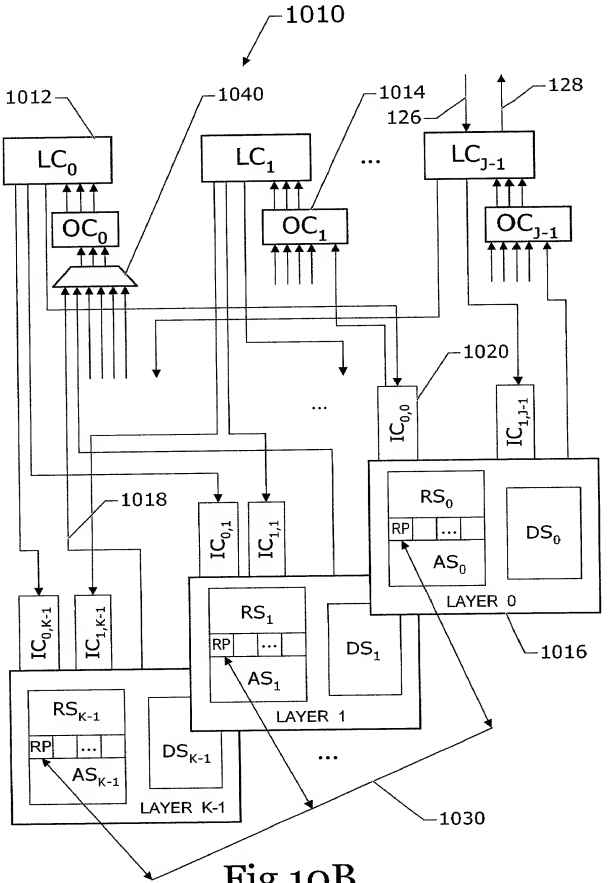
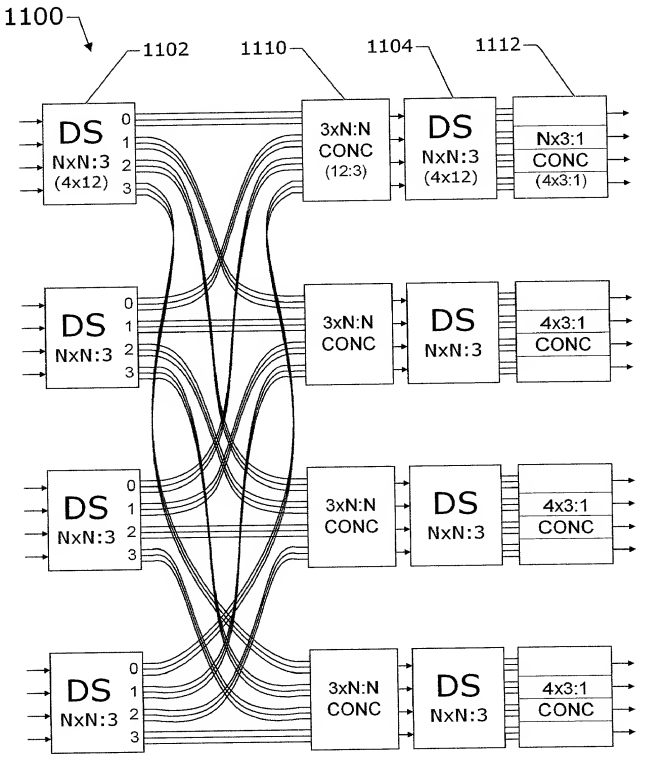
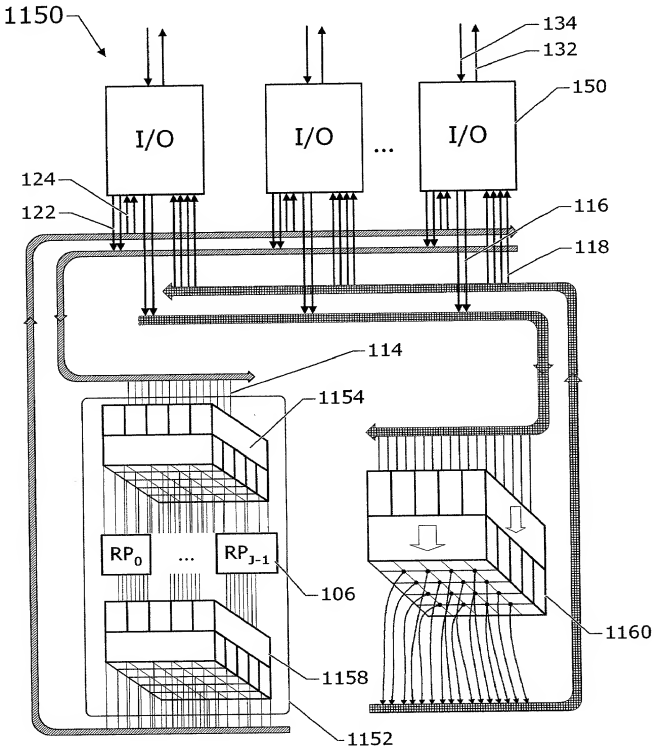


Fig 10B



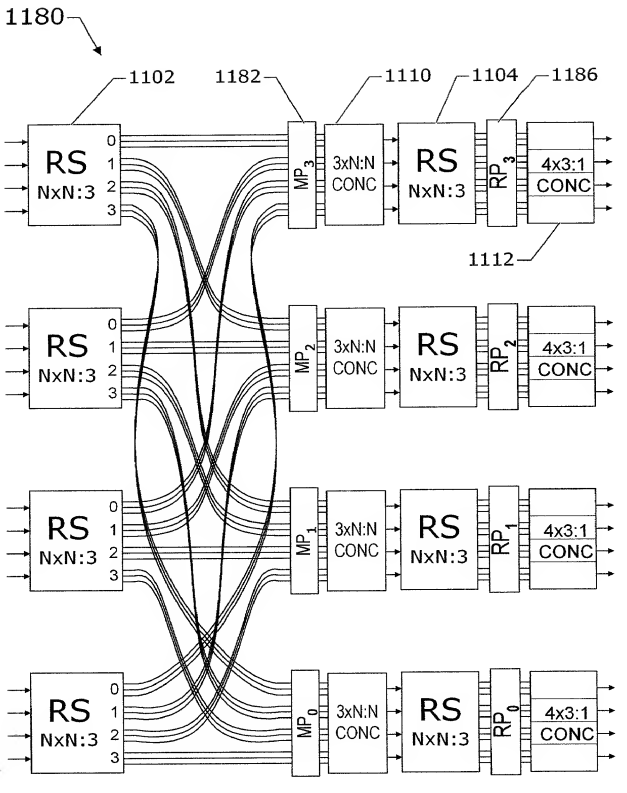
TWISTED CUBE DATA SWITCH

Fig 11A



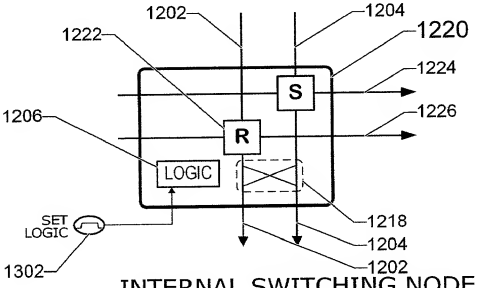
TWISTED CUBE CONTROL & DATA SWITCHES

Fig 11B



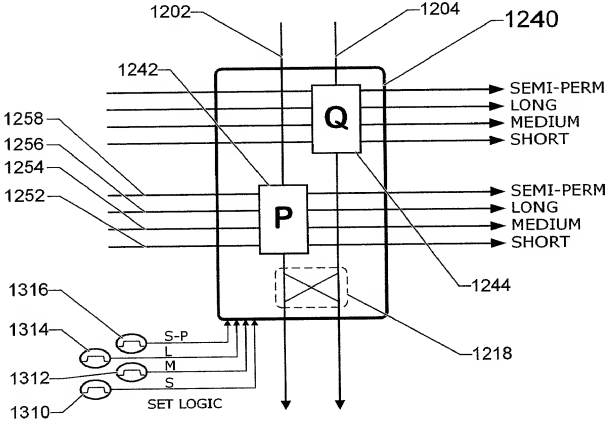
TWISTED CUBE CONTROL

Fig 11C



INTERNAL SWITCHING NODE

Fig 12A



MULTIPLE-LENGTH SWITCHING NODE

Fig 12B

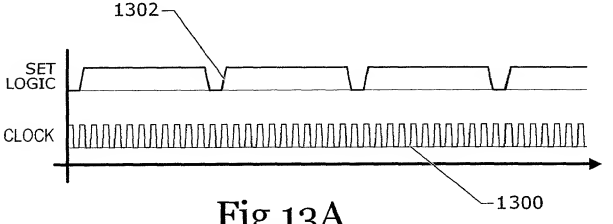


Fig 13A

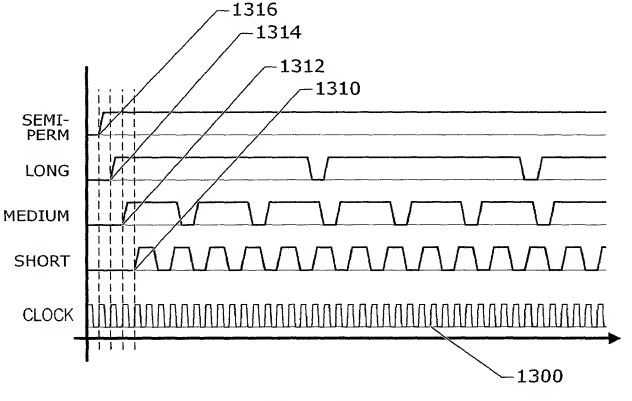


Fig 13B

MULTIPLE-LENGTH SWITCHING TIMING

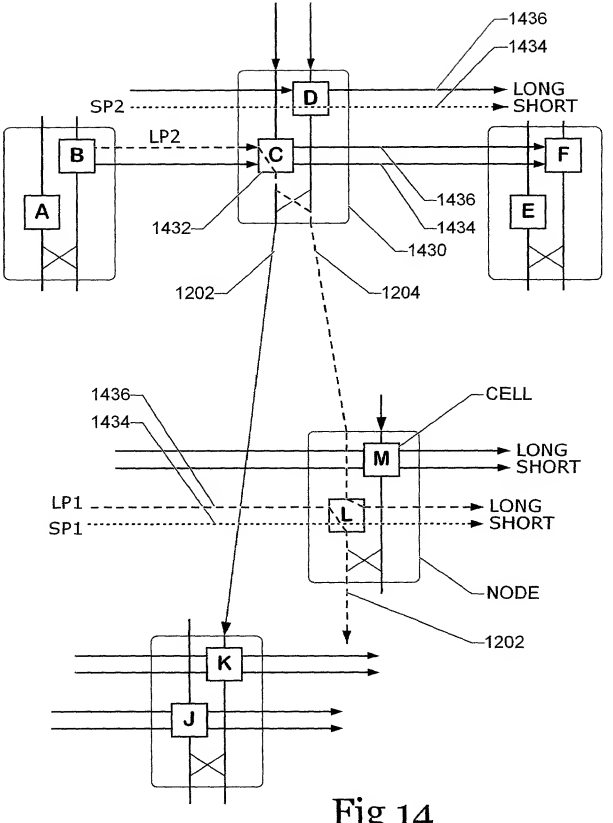


Fig 14

MULTIPLE-LENGTH SWITCH